

Call for Papers

Special Issue on Computing in Emerging Technologies

The potential alternatives to conventional CMOS transistors are being actively explored by device and technology community. There is a critical need to develop novel computing solutions to fully harness the potential of promising array of post-CMOS devices. Beyond CMOS systems may include emerging non-silicon devices, potentially integrated with CMOS electronics, and exploit advancements in heterogeneous integration. Designing complex beyond-CMOS systems require innovative approaches in circuit, architecture, and system design as well as associated modeling and design tools. To address this need, this special issue focuses on circuit, architecture, and system aspects of computing in beyond-CMOS electronics. These future beyond-CMOS systems would be characterized with: (1) computing with unconventional nanodevices with unique capabilities for logic and memory, e.g. nanowires, nanotubes, graphene, resistive and spin-based devices; (2) new logic and memory circuit styles; (3) new concepts on computing model and architecture to address the energy, reliability and security issues; (4) methods to reconfigure and/or mask faults at much higher rates than in CMOS; (5) heterogeneous system integration of hybrid technologies; and (6) design methods and tools.

Areas of interest include, but are not limited to:

- Nanoelectronic logic and memory circuits using post-CMOS electronics
- Novel computing platforms with nanodevices including non-Von Neumann computing
- Energy-efficient, reliable, and secure computing with unpredictable nanodevices
- Heterogeneous system with integration of hybrid technologies
- Design methods and tools for nanocircuits and nanosystems

Prospective authors should submit PDF versions of their papers following the instructions provided on the JETCAS website: <http://jetcas.polito.it>. The template files for LaTeX and Word are available for download from <http://www.ieee.org/pubs/authors.html>.

Guest Editors

- Saibal Mukhopadhyay, Georgia Tech
Email: saibal@ece.gatech.edu
- Hillery Hunter, IBM Research
Email: hhunter@us.ibm.com
- Kaushik Roy, Purdue University
Email: kaushik@ecn.purdue.edu
- Swarup Bhunia, Case Western Reserve University
Email: skb21@case.edu

Important Dates:

Paper submission: March 1, 2014
First round of reviews completed: June 15, 2014
Revised manuscripts due: August 1, 2014
Notification of acceptance: September 1, 2014
Final manuscripts due date: September 15, 2014