

IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS

CALL for PAPERS NEXT-GENERATION DELTA-SIGMA CONVERTERS

Guest editors

Jose M. de la Rosa	jrosa@imse-cnm.csic.es	Inst. of Microelectronics of Seville, IMSE-CNM (CSIC/Univ. of Seville)
Kong-Pang Pun	kppun@ee.cuhk.edu.hk	Dpt. of Electronic Engineering, The Chinese University of Hong Kong
Richard Schreier	richard.schreier@analog.com	Analog Devices Inc., Toronto
Shanthi Pavan	shanthi@ee.iitm.ac.in	Dpt. of Electrical Engineering, Indian Institute of Technology, Madras

Scope, purpose and submission procedure

Delta-Sigma ($\Delta\Sigma$) Analog-to-Digital Converters (ADCs) constitute one of the most efficient solutions to digitize signals in a number of very diverse application scenarios, while covering a wide conversion region of the resolution-versus-bandwidth plane. Their adaptability as well as their robustness and simplicity, has prompted the interest of more and more engineers over the last years, who usually consider $\Delta\Sigma$ techniques as the first choice for their industrial products or research applications.

However, technology downscaling towards advanced nanometer CMOS processes, as well as the aggressive specifications required in many consumer electronic products, demand for increasingly more and more efficient circuits and systems strategies in order to push the state-of-the-art on $\Delta\Sigma$ ADCs forward. Many of these strategies may require solving multidisciplinary problems, depending on the nature of the signals involved, environment interferences, measurement set-up conditions, etc.

In this scenario, this Special Issue aims to provide JETCAS readers with a detailed overview of the most relevant and emerging strategies and circuits/systems solutions, which are in the frontiers of $\Delta\Sigma$ conversion techniques, in terms of energy efficiency, frequency range and scalability to advanced nanometer CMOS. Among others, those sub-topics involving the development of new architectures and data conversion paradigms – like RF/GHz-range $\Delta\Sigma$ digitization for software defined radio, mostly-digital & scaling-friendly time-to-digital conversion, ultra-low-power amplifier-less loop-filter solutions, ultra-high-speed hybrid $\Delta\Sigma$ /Nyquist-rate implementations – as well as the implications derived from the integration of these techniques in next-generation mainstream technologies, are within the scope of this special issue, as detailed in the list of topics of interest.

Topics of interest

Among others, the following research topics will be addressed:

- Emerging applications of $\Delta\Sigma$ modulators
- RF and ultra-high speed (GHz-range) $\Delta\Sigma$ digitization
- Ultra-low power $\Delta\Sigma$ converters for, e.g. medical applications
- Power-efficient amplifier-less $\Delta\Sigma$ modulators
- Mostly digital, digital-assisted & scaling-friendly $\Delta\Sigma$ circuit techniques
- Reconfigurable & circuit-sharing $\Delta\Sigma$ circuits and systems
- Time-coded quantization and time-to-digital $\Delta\Sigma$ conversion
- Hybrid $\Delta\Sigma$ /Nyquist-rate (SAR, Pipeline...) ADCs
- CMOS integration strategies at advanced (< 40 nm) nodes

Submission guidelines

Prospective authors are invited to submit their manuscripts following the instructions for authors provided on the JETCAS submission website. The submitted manuscript should contain at least a 50% of new (previously unpublished) non-obvious technical material and needs to be prepared following the authors' guidelines for IEEE JETCAS manuscripts, which can be found at <http://jetcas.polito.it>.

Important dates

- | | |
|-------------------------------------|--------------------------|
| • Manuscript submissions due | May 3, 2015 |
| • First round of reviews completed | July 10, 2015 |
| • Revised manuscripts due | August 17, 2015 |
| • Second round of reviews completed | September 7, 2015 |
| • Final manuscripts due | October 2, 2015 |