

Special Issue on Robust and Energy-Secure Systems - Call for Papers -

The “power wall” has forced chip designers and system architects to integrate novel power and thermal management control loops into systems to enable smaller margins between nominal and worst-case operating points. These management protocols create new challenges for chip and system designers. Examples include control loop stability, robustness of the management protocols, potential security vulnerabilities in integrated control loops and management firmware, and system security and safety challenges triggered by violations of energy, reliability, power or thermal limits.

We have coined the term “robust and energy-secure systems” to cover the broad range of research being pursued within industry and academia to ensure reliable and secure operation of systems with integrated power, reliability, and thermal management control loops.

Through this JETCAS special issue, we seek novel research papers on holistic approaches to designing emerging on-chip control systems. We solicit papers in the areas of energy/power/thermal management, reliability, and security to provide a comprehensive view of the hardware and software aspects of Robust and Energy-Secure Systems.

Areas of interest include, but are not limited to:

- Holistic cross-layer energy, power, thermal and reliability management solutions
- Robustness of system energy/power/thermal/reliability management: verification, validation and design for verification
- Reliability and security holes exposed by energy/power/thermal management protocols
- Guarded, two-level management protocols for safety, security and low verification complexity
- Architectural implications of and system software support for robust energy/power/thermal management
- Reliability and security issues in emerging low-power memory technologies
- Power- and thermal-based side-channel attacks

Prospective authors should submit PDF versions of their papers following the instructions provided on the JETCAS web-site: <http://jetcas.polito.it/general.html>. Submitted manuscripts should not have been previously published nor should they be currently under consideration for publication elsewhere. Manuscripts will undergo a peer review process according to the standard IEEE publication policy.

Guest Editors:

- Augusto Vega, IBM Research
Email: ajvega@us.ibm.com
- Simha Sethumadhavan, Columbia University
Email: simha@cs.columbia.edu
- Subhasish Mitra, Stanford University
Email: subh@stanford.edu

Important Dates:

- Paper submission: January 31, 2014
- First round of reviews completed: February 21, 2014
- Revised manuscripts due: March 4, 2014
- Notification of acceptance: March 25, 2014
- Final manuscripts due date: April 1, 2014

Supporting Committee:

- Dimitris Gizopoulos, University of Athens (Greece)
- Ramón Canal, UPC Barcelona (Spain)
- Hiroshi Nakamura, University of Tokyo (Japan)
- Pradip Bose, IBM Research (United States)
- Alper Buyuktosunoglu, IBM Research (United States)
- Hiroshi Sasaki, Kyushu University (Japan)