

IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS

CALL for PAPERS

Special Issue on Emerging Topics in Multiple-Valued Logic and Applications

Guest editors

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Scope, purpose and submission procedure

Multiple-valued logic (MVL) is the broad field of study of circuits and systems in which information is carried by more than two values, or where information is represented in unconventional, i.e., non-binary-weighted ways. There have been many recent MVL innovations that are relevant to circuit and system design, including: memory cells storing multiple bits/cell, MVL approaches to the design and modeling of nanotechnologies, multiple-valued decision diagrams, and MVL approaches to reversible and quantum computing. For this Special Issue, you are invited to submit an article on an emerging subject in the area of MVL. Articles should be addressed primarily to the diverse readership of *JETCAS* and must focus on one of the emerging aspects of the field.

Prospective authors should submit PDF versions of their papers following the instructions provided on the *JETCAS* web-site: <http://jetcas.polito.it/general.html>. Submitted manuscripts should not have been previously published nor should they be currently under consideration for publication elsewhere. Manuscripts will undergo a peer review process according to the standard IEEE publication policy.

Topics of interest

- *Multi-bit per cell logic & memory*
- *Multiple-Valued Decision Diagrams applied to circuit/system design/analysis*
- *MVL Aspects of Nanotechnology, including carbon nanotube design*
- *Quantum Computing/Reversible Computing*

Important dates

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| • Manuscript submissions due | February 1, 2015 |
| • First round of reviews completed | May 1, 2015 |
| • Revised manuscripts due | June 1, 2015 |
| • Second round of reviews completed | July 1, 2015 |
| • Final manuscripts due | August 1, 2015 |

Request for information

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